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10/072,872	02/12/2002	Yoshie Kanamori	100021-00069	2414

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,872	KANAMORI ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8-20,22-25 and 27-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8-20,22-25 and 27-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/21/03 has been entered.

Response to Amendment

2. The amendment filed on 8/21/03 has received and entered in the case based on the RCE filed on 10/9/03.

3. Upon further reconsideration, the allowable claims 1, 3, 8-10, 16-20, 22, 27-29 and 35-37 in the last office action are now withdrawn for the reasons set forth below in this office action.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the differential amplifier which including a third transistor for keeping a minute current to flow through said first and second transistors, and wherein the third transistor doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit, and also including a fourth transistor as recited in claims 4-6 and 23-25; the differential amplifier which including a third transistor for keeping a minute current to flow through said first and second transistors, and wherein the third transistor doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit, and also including a fifth transistor as recited in claims 11 and 30; the differential amplifier which including a third transistor for

keeping a minute current to flow through said first and second transistors, and wherein the third transistor doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit, and also including a sixth transistor as recited in claims 12-13 and 31-32; the differential amplifier which including a third transistor for keeping a minute current to flow through said first and second transistors, and wherein the third transistor doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit, and also including a seventh transistor as recited in claims 14 and 33; and the differential amplifier which including a third transistor for keeping a minute current to flow through said first and second transistors, and wherein the third transistor doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit, and also including an eighth transistor as recited in claims 15, 34, 38 and 39 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 1, 8, 17, 19, 27 and 36 are objected to because of the following informalities:

In claim 1, line 10, it appears that "double as a transistor" be changed to --also-- since it is not clear what exactly "double as a transistor" means.

In claim 1, it is not clear what exactly "by said differential amplifier" on line 11 means, and it appears that "by said" on line 11 should be changed to --for said--.

In claim 8, line 3, "a predetermined drive current" should be changed to --the drive current-- to avoid unclear antecedent basis because independent claim 1 already recites "a drive current".

In claim 17, it appears that "double as a transistor" on line 14 be changed to --also--, and "by said" on line 11 should be changed to --for said-- for the same reason as discussed in claim 1 above.

In claim 19, line 4, "the outputting" should be changed to --and outputting--.

In claim 27, line 3, "a predetermined drive current" should be changed to --the drive current-- to avoid unclear antecedent basis because independent claim 17 already recites "a drive current".

In claim 36, line 5, "receiving the differential signal" should be deleted to avoid a confusion in the claim since the claim later on recites that the differential amplifier circuit receives the outputs (the inter-symbol interference removed differential signal) of the equalizer circuit (see lines 13-14 of the claim).

Appropriate correction and/or clarification is required for the above objections.

6. Claims 20 and 37 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. In this case, claims 20 and 37 fail to further limit the semiconductor integrated circuit of the previous claims 19 and 36, respectively.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 4-6, 14, 15, 23-25, 33, 34, 38 and 39 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

With respect to claims 4-6 and 23-25, the disclosure does not disclose any differential amplifier circuit which includes a third transistor for keeping a minute current to flow and also for supplying a drive current at the time of signal determination, and also including a fourth transistor as recited in these claims. Note that disclosure discloses a third transistor (30', Figure 11A) for keeping a minute current to flow through said first and second transistors, and wherein the third transistor (30', Figure 11A) doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit. However, Figure 11A does not show a fourth transistor for supplying a drive current, wherein the fourth transistor is connected in parallel with the third transistor. Thus, the disclosure does not disclose any differential amplifier circuit which includes a third transistor for keeping a minute current to flow and also for supplying a drive current at the time of signal determination, and also including a fourth transistor as recited in these claims.

With respect to claims 14 and 33, the disclosure does not disclose any differential amplifier circuit which includes a third transistor for keeping a minute current to flow and also for supplying a drive current at the time of signal determination, and also including a seventh

transistor as recited in the claim. Note that the disclosure discloses a third transistor (30', Figure 11A) for keeping a minute current to flow through said first and second transistors, and wherein the third transistor (30', Figure 11A) doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit. However, Figure 11A does not show a seventh transistor as recited in the claims. Thus, the disclosure does not disclose any differential amplifier circuit which includes a third transistor for keeping a minute current to flow and also for supplying a drive current at the time of signal determination, and also including a seventh transistor as recited in the claim.

With respect to claims 15, 34, 38 and 39, the disclosure does not disclose any differential amplifier circuit which includes a third transistor for keeping a minute current to flow and also for supplying a drive current at the time of signal determination, and also including an eighth transistor as recited in the claim. Note that the disclosure discloses a third transistor (30', Figure 11A) for keeping a minute current to flow through said first and second transistors, and wherein the third transistor (30', Figure 11A) doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit. However, Figure 11A does not show an eighth transistor as recited in these claims. Thus, the disclosure does not disclose any differential amplifier circuit which includes a third transistor for keeping a minute current to flow and also for supplying a drive current at the time of signal determination, and also including an eighth transistor as recited in these claims.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 1, 3-6, 8-20, 22-25, and 27-39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1, "minute" on line 7 is a relative term and the specification does not specifically indicate at which current value is considered to be "minute current". Therefore, it is not know how large/small of a current value to meet the limitation "minute current" in the claim. Note that the same problem also exists in claims 17, 36, 38 and 39.

Claims 2-6, 8-16, 18-20, 22-25, 27-35, and 37 are indefinite because they include the indefinite problem as recited in claims 1, 17, and 36 above.

Claim 4 is indefinite because the claim is misdescriptive since there is no such circuit corresponding to claim 4. Note that the independent claim 1 reads on Figure 11A, i.e., a third transistor (30', Figure 11A) for keeping a minute current to flow through said first and second transistors, and wherein the third transistor (30', Figure 11A) doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit. However, Figure 11A does not show a fourth transistor for supplying a drive current, wherein the fourth transistor is connected in parallel with the third transistor. Furthermore, independent claim 1 cannot be read on any of the other circuits (except Figure 11A) because no such third transistor for keeping the minute current to flow and wherein the third transistor doubles a transistor for supplying the drive current at the time of signal determination, so claim 4 cannot be read on any of the circuits.

Claims 5 and 6 are indefinite because they include the indefiniteness of claim 4, i.e., there is no such fourth transistor.

Claim 14 is indefinite because the claim is misdescriptive since there is no such circuit corresponding to claim 14. Note that the independent claim 1 reads on Figure 11A, i.e., a third transistor (30', Figure 11A) for keeping a minute current to flow through said first and second transistors, and wherein the third transistor (30', Figure 11A) doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit. However, Figure 11A does not show a seventh transistor as recited in claim 14. Furthermore, independent claim 1 cannot be read on any of the other circuits (except Figure 11A) because none of the Figures (except Figure 11A) shows such third transistor for keeping the minute current to flow and wherein the third transistor doubles a transistor for supplying the drive current at the time of signal determination, so claim 14 cannot be read on any of the circuits.

Claim 15 is indefinite because the claim is misdescriptive since there is no such circuit corresponding to claim 15. Note that the independent claim 1 reads on Figure 11A, i.e., a third transistor (30', Figure 11A) for keeping a minute current to flow through said first and second transistors, and wherein the third transistor (30', Figure 11A) doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit. However, Figure 11A does not show an eighth transistor as recited in claim 15. Furthermore, independent claim 1 cannot be read on any of the other circuits (except Figure 11A) because none of the Figures (except Figure 11A) shows such third transistor for keeping the minute current to flow and wherein the third transistor doubles a transistor for supplying the drive current at the time of signal determination, so claim 15 cannot be read on any of the circuits. Insofar as understood, the disclosure does not disclose any differential amplifier circuit which includes a third transistor for keeping a minute current to flow and also for supplying a drive

current at the time of signal determination, and also including an eighth transistor as recited in the claim.

Claims 23-25 are indefinite because these claims are misdescriptive for the same reasons as discussed in claims 4-6 above.

Claim 33 is indefinite because it is misdescriptive for the same reasons as discussed in claim 14 above.

Claims 34, 38 and 39 are indefinite because they are misdescriptive for the same reasons as discussed in claim 15 above.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 1, 3, 8-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admitted prior art (each of Figures 2-4) in view Itou (USP 5,903,513).

With respect to claim 1, each of the Figures 2-4 of the applicant's admitted prior art shows a differential sense amplifier circuit which includes: a latch unit (111, 112, 121, 122); and a differential input portion (101, 102) comprises a first transistor (101) and a second transistor (102); and a current device (130 including a third transistor (130). Each of the Figures 2-4 of the applicant's admitted prior art does not disclose that the third transistor (130) for keeping a minute current to flow through the differential input portion, and also for supplying a drive current at the time of signal determination for the differential amplifier circuit. However, Figure

7 of the Itou reference disclose a differential amplifier circuit (61) which includes current device (74) including a third transistor (71) for keeping a minute current (i.e., when clock CLKH is low, transmission gate 72 is on so the gate of transistor 71 receives the lower reference voltage VaL, so there is a smaller current (minute current) to flow through the differential amplifier) to flow through the differential input portion of the differential amplifier, and also for supplying a drive current at the time of signal determination for the differential amplifier (i.e., at the time of signal determination which is when clock CLKH is Hi, transmission gate 73 is on so the gate of transistor 71 receives the higher reference voltage VaH, so transistor 71 supplies a larger current (drive current) for the differential amplifier) for the purpose of controlling the gain of the differential amplifier (see lines 6-53 of Col. 12 of Itou). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the differential amplifier in each of the Figures 2-4 of the applicant's admitted prior art to replace the current device (130) by the current device (74, Figure 7 of Itou) as taught by the Itou reference for the purpose of controlling the gain of the differential amplifier. Thus, each of these combination/modification meets all the limitations of claim 1 because the third transistor (transistor 71 in the above combination/modification) for keeping a minute current to flow (when CLKH is low, gate of transistor 71 receives a lower reference VaL as discussed above) and also for supplying a drive current at the signal determination for the differential amplifier (when CLKH is Hi, gate of transistor 71 receives a higher reference VaL as discussed above). Note that the clock signal CLKH in this modifications/combinations would be the clock signal for overall circuit (i.e., the clock signal CLKH in Figure 7 of the Itou reference, and the clock CK in each of

the Figures 2-4 of the applicant's admitted prior art are now the same clock signal, called CLKH).

With respect to claim 3, it is seen in each of the above modifications/combinations that the third transistor turns off the minute current flowing through the first and second transistor upon deactivation of the differential amplifier. This is because upon deactivation (power off) of the differential amplifier, there is no power supplied to the circuit and therefore the third transistor is off.

With respect to claim 8, it is seen in each of the above modifications/combinations that a first control signal (signal at the gate of transistor 71 in Figure 7 of the Itou reference in the above combination/modification as discussed) is supplied to the control electrode of the third transistor (71) is set to a level (VaH) for supplying the drive current at the time of the signal determination (when CLKH is Hi), while causing the minute current to flow through the first and second transistors at other than the time of signal determination (i.e., when CLKH is not Hi) during the operation of the differential amplifier.

With respect to claim 9, each of the Figures 2-4 of the applicant's admitted prior art in the each of the above combinations/modifications, respectively, shows the latch (111, 112, 121, 122) including a first inverter (111, 112) and a second inverter (121, 122) being cross-coupled to each other.

With respect to claim 10, Figure 3 of the applicant's admitted prior art in the above combination/modification (Figure 3 of the applicant's admitted prior art in view of Figure 7 of Itou) shows additional transistors (110, 120) connected in parallel with transistors (111, 121), respectively; and the second electrode (the drains of 101 and 102) of each of the first and second

transistors (101, 102) is held at a predetermined level at other than the time of signal determination during the operation of the differential amplifier (because the structure of the above combination/modification is same as applicant's invention, so the functional limitation is met).

With respect to claim 11, Figure 2 of the applicant's admitted prior art in the above modification/combination (Figure 2 of the applicant's admitted prior art in view of Figure 7 of Itou) shows a fifth (140) transistor for shoring the second electrodes of the first and second transistors (101 and 102) in accordance with a second control signal (the clock signal).

With respect to claim 12, Figure 3 of the applicant's admitted prior art in the above modification/combination (Figure 3 of the applicant's admitted prior art in view of Figure 7 of Itou) shows a sixth transistor (150) for connecting the second electrodes of the first and second transistors (101 and 102) together, wherein the sixth transistor has its gate connected to a predetermined voltage (AVD).

With respect to claim 13, the combination of Figure 3 of applicant's admitted prior art and Figure 7 of the Itou reference as discussed above meets the limitation "wherein said differential input signal is at CML level" (see the description of Figure 3 of applicant's admitted prior art on lines 5-9, page 10, of the instant specification).

With respect to claim 14, the combination of Figure 4 of applicant's admitted prior art and Figure 7 of the Itou reference as discussed above shows a seventh transistor (160) inserted between two nodes (q, qx) for retrieving a differential output signal (q, qx), the seventh transistor (160) shorting the two nodes in accordance with a third control signal (the clock signal).

With respect to claim 16, it is seen that the differential amplifier in the above combination/modification is a differential sense amplifier circuit of strong arm latch type (the differential sense amp in the above combination/modification includes a latch portion as applicant's invention).

13. Claims 17, 18, 22, 27-33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (each of Figures 2-4) in view of Itou (UPS 5,903,513) and Oklobdzija et al. (USP 6,232,810).

With respect to claim 17, each of the above combinations/modifications (each of Figures 2-4 of applicant's admitted prior art and the Figure 7 of the Itou reference as discussed in section 10 above with regard to claim 1) discloses a semiconductor device having a differential amplifier circuit, and a clock source (inherently, e.g., whichever source that is used to generate the clock signal in the above combination/modification) generating a clock (CLKH) and supplying the generated clock (CLKH) to the differential amplifier circuit, wherein the differential amplifier circuit includes a latch unit and a differential input portion, wherein: the differential input portion (101, 102) including a first transistor (101) and a second transistor (102) each having a first electrode (the electrode connected to transistor 130), a second electrode (the electrode connected to transistors 112 or 122) and a control electrode (gate); the control electrodes of the first and second transistors are supplied with a differential input signal (d, dx); a third transistor (71 as taught in Figure 7 of Itou which is discussed the above combination/modification with regard to claim 1) for keeping the minute current to flow through the first (101) and second (102) transistors, and also for supplying a drive current at the time signal determination (i.e., when CLKH is Hi) for the differential amplifier. While each of the above combinations (as discussed

in section 10 with regard to claim 1) fails to disclose each of the semiconductor devices includes a latch circuit latching an output signal of the differential amplifier circuit, the Oklobdzija et al. reference discloses that an SR latch circuit connected to the output of the differential sense amplifier to latch the output of the differential sense amplifier for the well-known purpose of making a D flip-flop circuit (see Figures 1 and 3, lines 13-15 of Col. 1, and lines 11-12 of Oklobdzija et al.). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the differential sense amplifier in each of the above combinations (each of Figures 2-4 of the applicant's admitted prior art and Figure 7 of the Itou reference) with an SR latch circuit connected at the output of the differential sense amplifier for the purpose of making a D flip-flop circuit for use in digital systems, such as processors, digital signal processors and memories. Thus, the limitation of claim 17 is met.

With respect to claim 18, the combination/modification Figure 3 of applicant's admitted prior art and Figure 7 of the Itou reference, and the Oklobdzija et al. reference meets all the limitations of this claim, e.g., the semiconductor integrated circuit device is a receiving circuit (any circuitry that receives an input signal can be construed as a receiving circuit) of a signal transmission system (e.g., digital systems such as processors or memories that the differential D Flip-flop used in), the signal transmission system including a transmission circuit (inherently, e.g., whichever circuit that is used to generate the differential signal d and dx for inputting to the differential sense amplifier) outputting the differential signal, a signal transmission path (the wires connected between the output of the circuit that is used to generated differential signal d and dx to the input of the differential sense amplifier), and the receiving circuit receiving the differential signal through the signal transmission path (the wires).

With respect to claim 22, this claim is rejected for the same reason as discussed in claim 3 as discussed above.

With respect to claim 27, this claim is rejected for the same reason as discussed in claim 8 as discussed above.

With respect to claim 28, this claim is rejected for the same reason as discussed in claim 9 as discussed above.

With respect to claim 29, this claim is rejected for the same reason as discussed in claim 10 as discussed above.

With respect to claim 30, this claim is rejected for the same reason as discussed in claim 11 as discussed above.

With respect to claims 31 and 32, these claims are rejected for the same reason as discussed in claim 12 and 13, respectively, as discussed above.

With respect to claim 33, this claim is rejected for the same reason as discussed in claim 14 as discussed above.

With respect to claim 35, this claim is rejected for the same reason as discussed in claim 16 as discussed above.

Allowable Subject Matter

14. Claims 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if rewritten to overcome the indefinite problem set forth above in this office action.

Claim 19 would be allowed because the prior art of record fails to disclose or suggest, in combination with other limitations, an equalizer circuit which receiving the differential signal, removing an inter-symbol interference of the differential signal by a partial response detection, and outputting the inter-symbol interference removed differential signal to the differential amplifier circuit (see Figure 19).

Claim 20, includes all the limitation of allowable claim 19, so this claim would also be allowed once the claim is re-written in a proper form that includes all the limitation of claim 19.

15. Claims 36 and 37 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Claim 36 would be allowed for the similar reason as indicated in claim 19 above.

Claim 37 includes all the limitation of allowable claim 36, so this claim would also be allowed once the claim is re-written in a proper form that includes all the limitation of claim 36.

Response to Arguments

16. Applicant's arguments filed on 8/21/03 have been fully considered but they are not persuasive.

With Respect to The Drawings Objections:

Applicant argues that the fourth transistor recited in claims 4-6 and 23-25 is illustrated in the drawings, namely transistor 30 in Figures 8, 9, and 13-17. However, these Figures 8, 9, and 13-17 does not show the third transistor (which is required in the independent claims) for keeping the minute current to flow and also for supplying a drive current at signal determination for the differential amplifier. Note that 37 CFR 1.83(a) requires that the drawings must show every feature of the invention specified in the claims. Therefore the drawings must shows a

circuit which includes the third transistor for keeping the minute current to flow and also for supplying a drive current at signal determination for the differential amplifier, and also includes the fourth transistor as claimed in claims 4-6 and 23-25, or the feather of the fourth transistor must be canceled from the claims. No new matters should be entered. Note that the similar explanation also applied for the drawings fails to show the fifth transistor in claims 11 and 30, the sixth transistor in claims 12-13 and 31-32, the seventh transistor as recited in claims 14 and 33, and the eight transistor in claims 15, 34, 38 and 39.

Applicant further argues that the specification, on lines 24-28 of page 17, also teaches that transistor 4 maybe inserted between the drains of the differential inputs transistor 1 and 2 in the embodiment of Figure 11A. However, Figure 11A does not show transistor 4 connected between the drains of differential input transistors 1 and 2. Again, 37 CFR 1.83(a) requires that the drawings must show every feature of the invention specified in the claim.

With Respect to The 35 USC 112, Second Paragraph Rejections

With respect to claims 4-6 and 23-25, applicant argues that, an example of the fourth transistor recited in claim 4 is illustrated by transistor 30 shown in Figures 8-9 and 13-17. However, these Figures 8, 9, and 13-17 does not show the third transistor (which is required in the independent claims) for keeping the minute current to flow and also for supplying a drive current at signal determination for the differential amplifier. Note that the third transistor as recited in the claim is shown in Figure 11A, but Figure 11A does not show the fourth transistor. Note that the same reasons also applied to claims 14, 15, 33 and 34.

Conclusion

17. Because claims 4-6, 15, 23-25, 34, 38 and 39 are not disclosed as discussed above with respect to the rejection under 35 U.S.C. 112, the scope (metes and bounds) of these claims cannot be determined so no prior art can be applied to these claims at this time.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (703) 308-6063. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (703) 308-4876. The fax number for this group is (703) 872-9306.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

LN
Date: November 25, 2003

Long Nguyen
Art Unit: 2816